

GodNeedle-6 家族

FPGA 封装说明

PK206



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版本说明

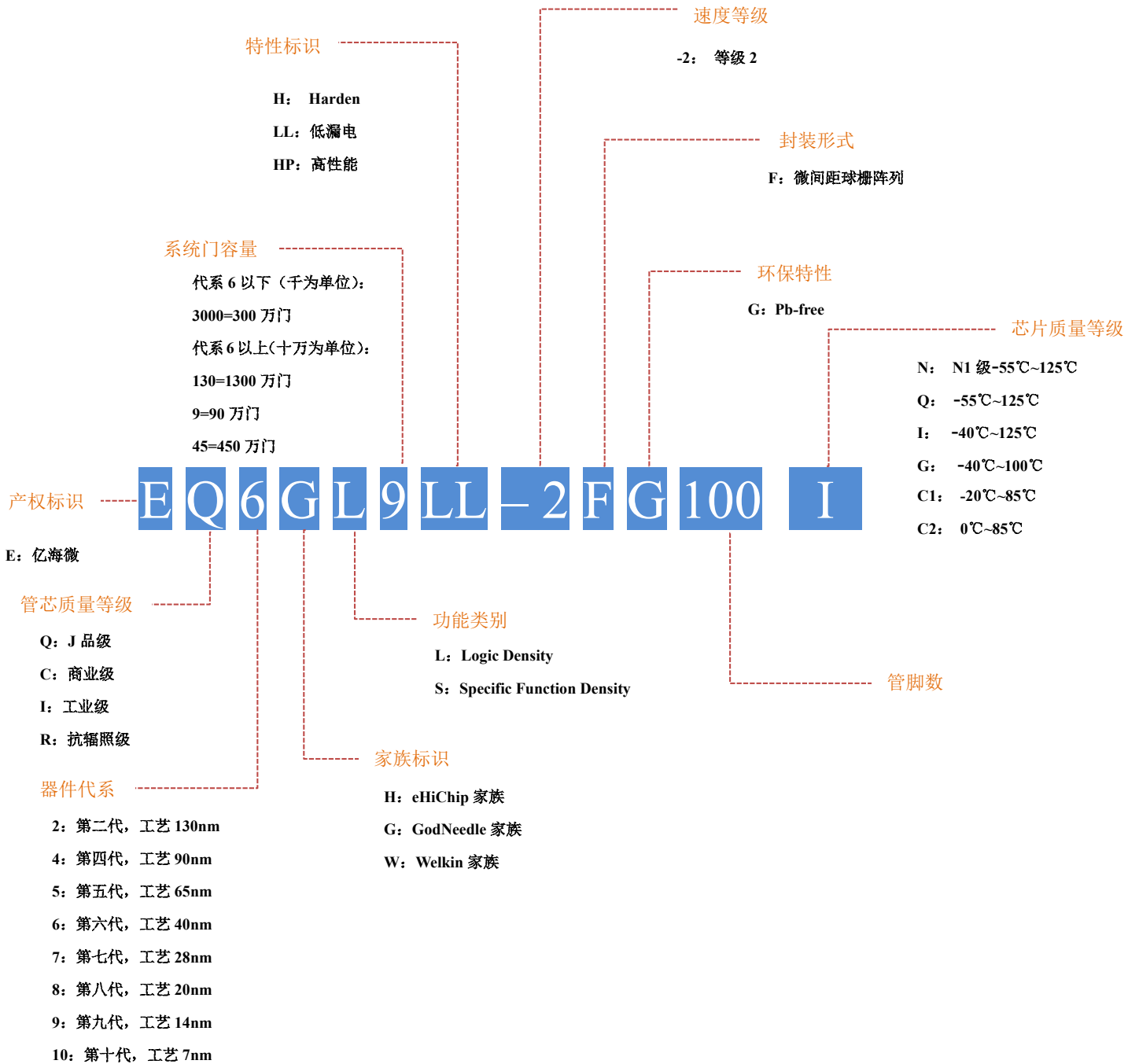
日期	版本	修订
2021.7.7	2021.1.1	新编
2021.8.11	2021.1.2	修改产品型号命名格式
2021.8.27	2021.1.3	增加封装型号
2021.9.10	2021.1.4	修改格式
2021.10.29	2021.1.5	修改内容
2021.11.9	2021.1.6	修改芯片质量等级

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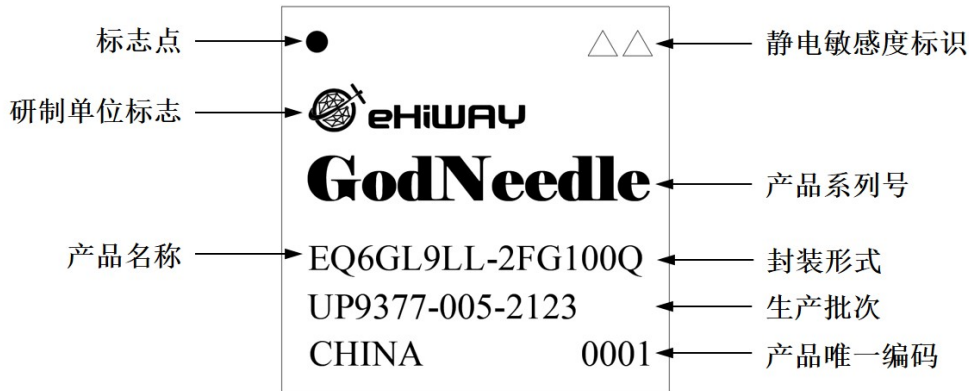
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1 FG100 封装

1.1 产品型号命名规则



1.2 封装丝印信息



1.3 封装尺寸

EQ6GL9 器件采用 100 引线的塑料球栅阵列封装，外形代号为 FG100，外形尺寸如图 1 和表 1 所示。

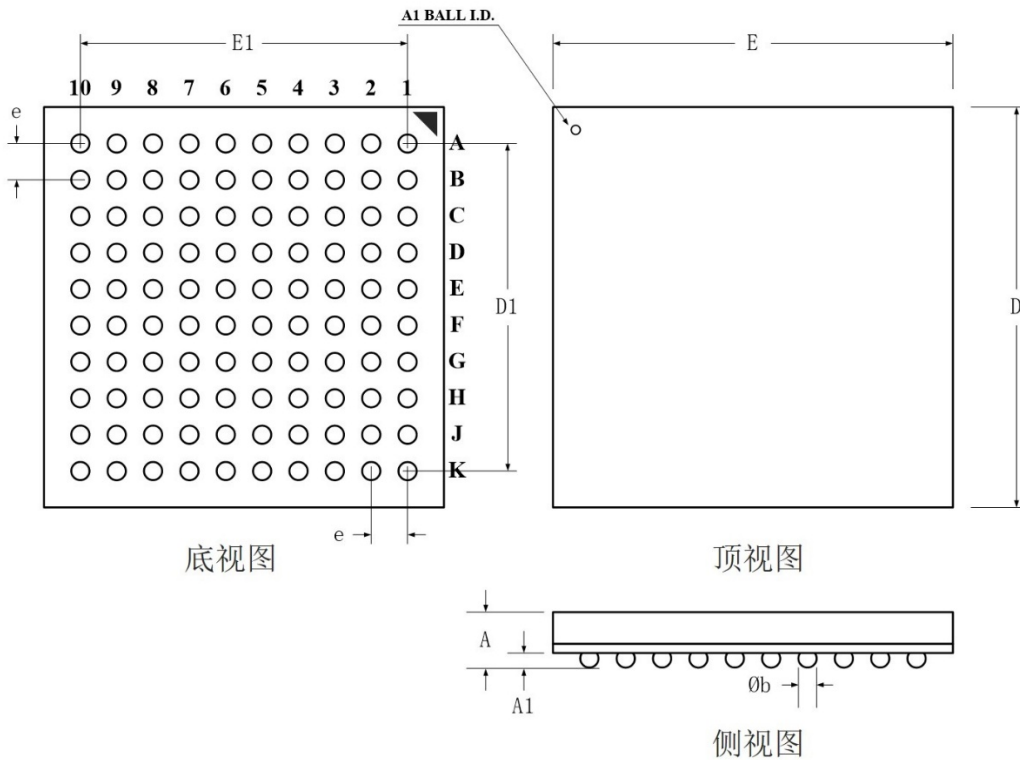


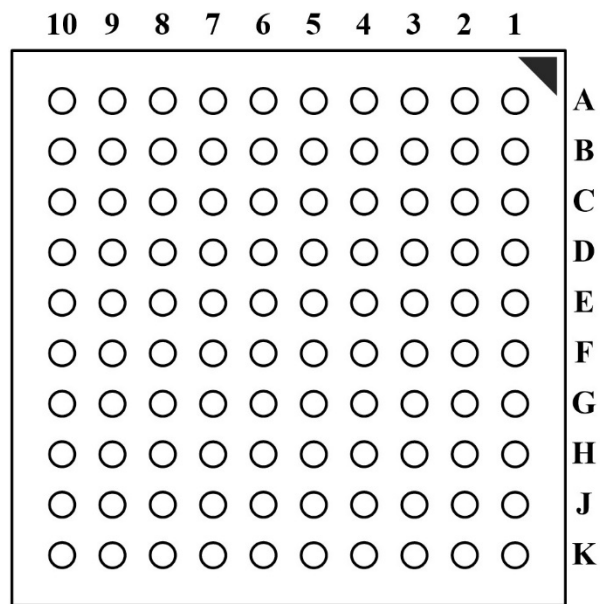
图 1 FG100 封装外型尺寸

表 1 FG100 封装外形尺寸

尺寸符号	数值 (单位毫米)		
	最小	公称	最大
A	1.30	1.50	1.70
A1	0.30	0.50	0.70
D	—	11.00	—
E	—	11.00	—
D1	—	9.00	—
E1	—	9.00	—
Øb	0.40	0.55	0.70
e	—	1.00	—

1.4 引出端排列

引出端排列规则如图 2 所示，具体管脚定义参见附录 A。

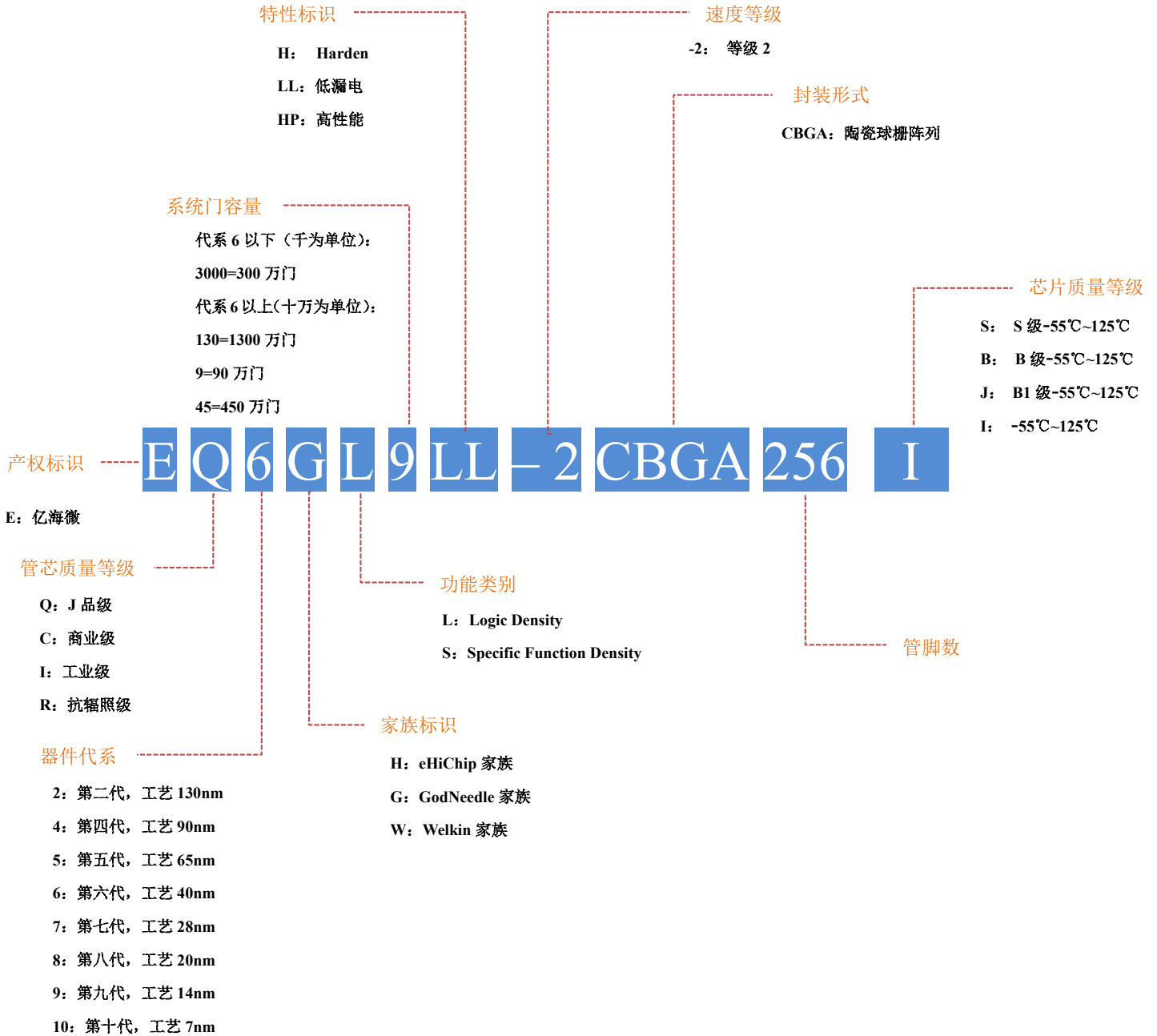


底视图

图 2 引出端排列示意图

2 CB256 封装

2.1 产品型号命名规则



2.2 封装尺寸

EQ6GL9 器件采用 256 引线的陶瓷球栅阵列封装，外形代号为 CBGA256，外形尺寸如图 3。

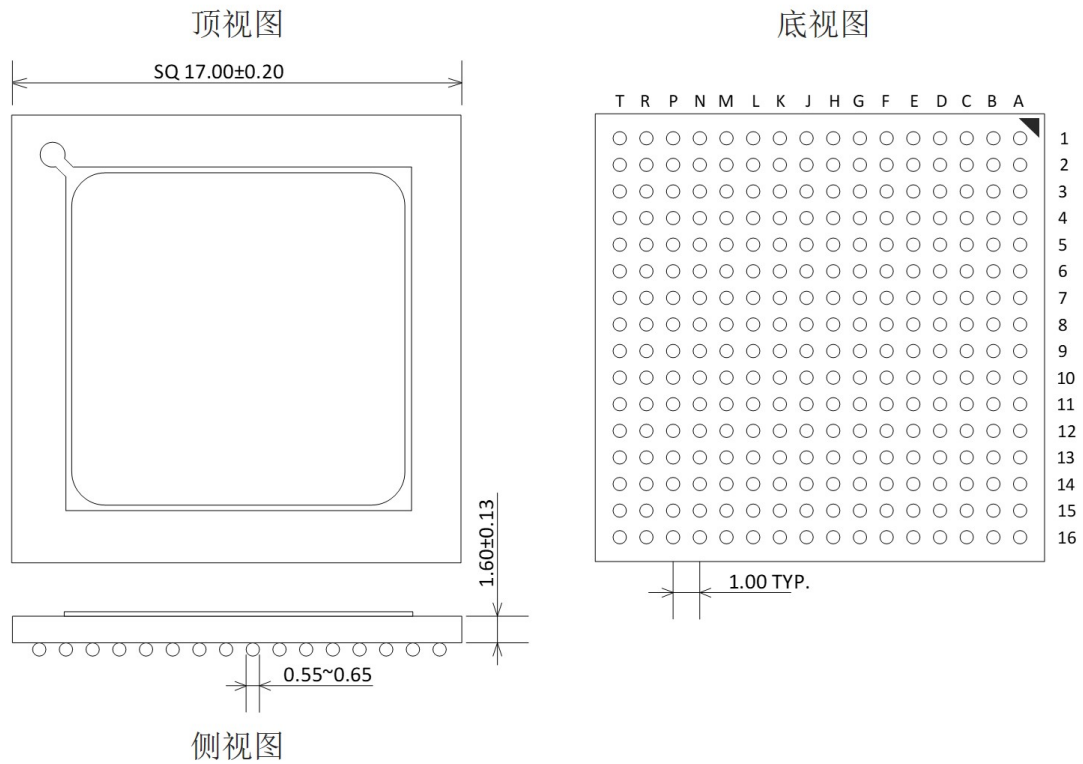
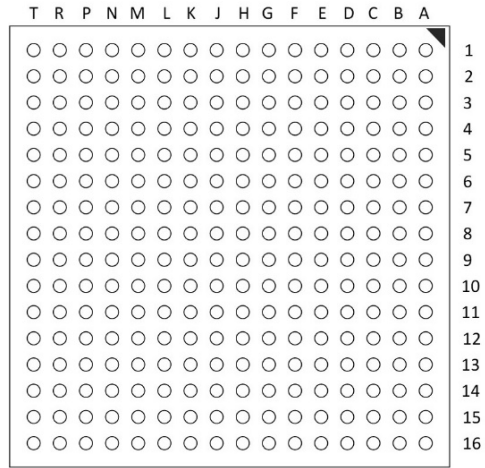


图 3 CBGA256 封装外型尺寸

2.3 引出端排列

引出端排列 (BOTTOM VIEW) 规则如图 4 所示，具体管脚定义参见附录 B。

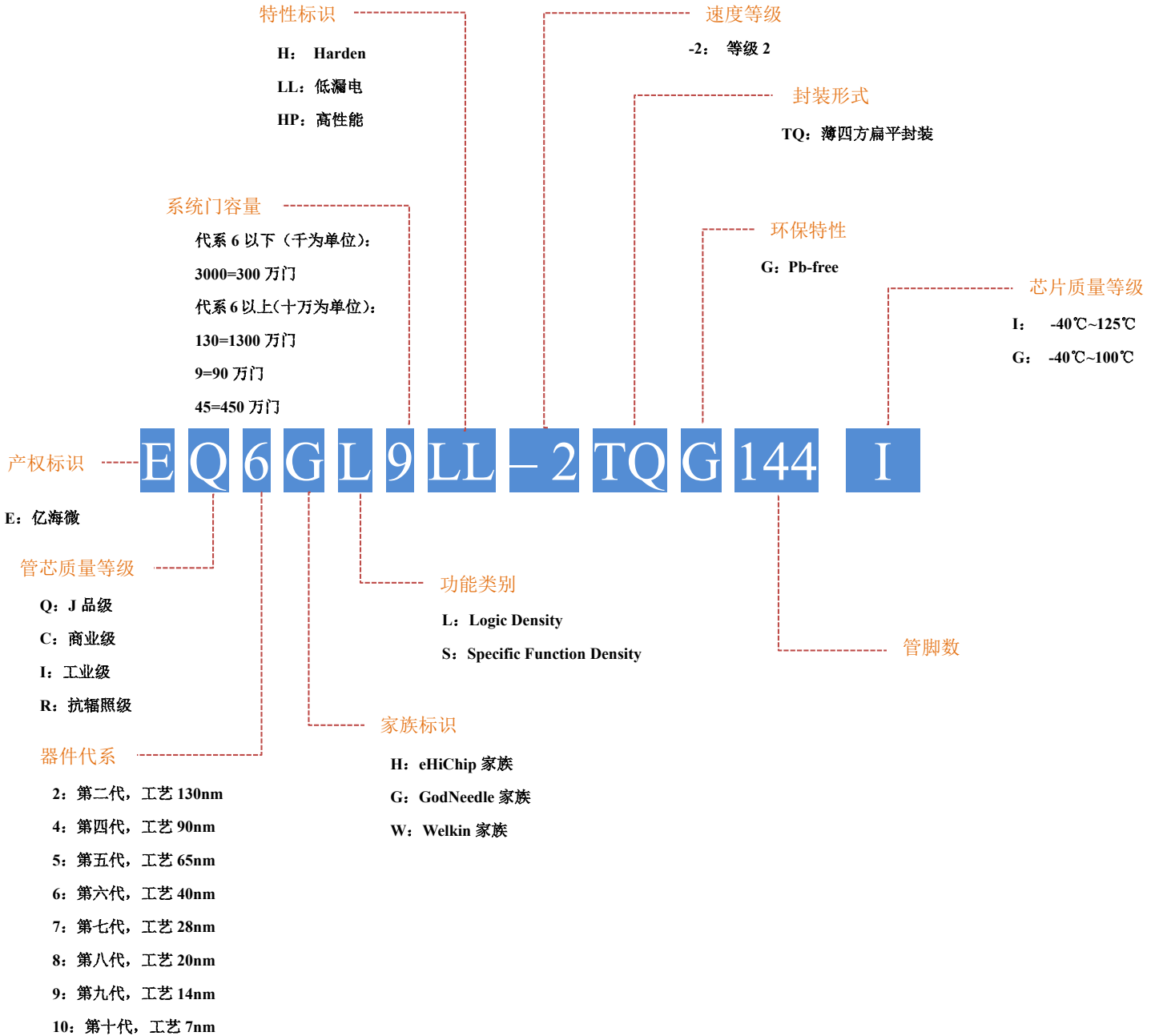


底视图

图 4 引出端排列示意图

3 TQG144 封装

3.1 产品型号命名规则



3.2 封装尺寸

EQ6GL9LL 器件采用 144 个引脚数的四方扁平封装，外形代号为 TQG144，外形尺寸如图 5 所示。

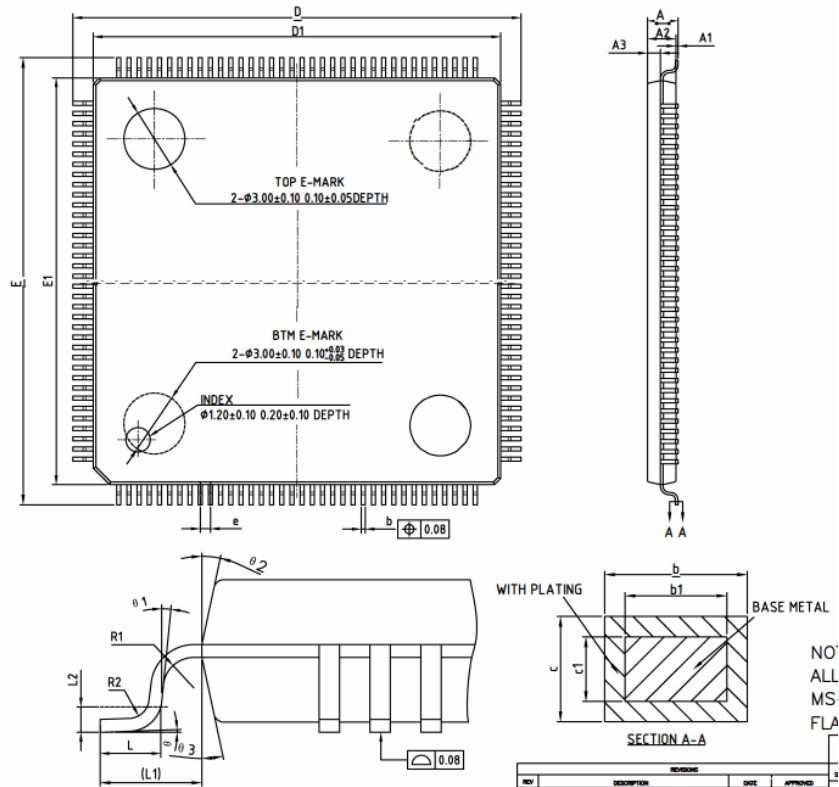


图 5 TQG144 封装外型尺寸

3.3 引出端排列

引脚排列规则如图 6 所示，具体管脚定义参见附录 C。

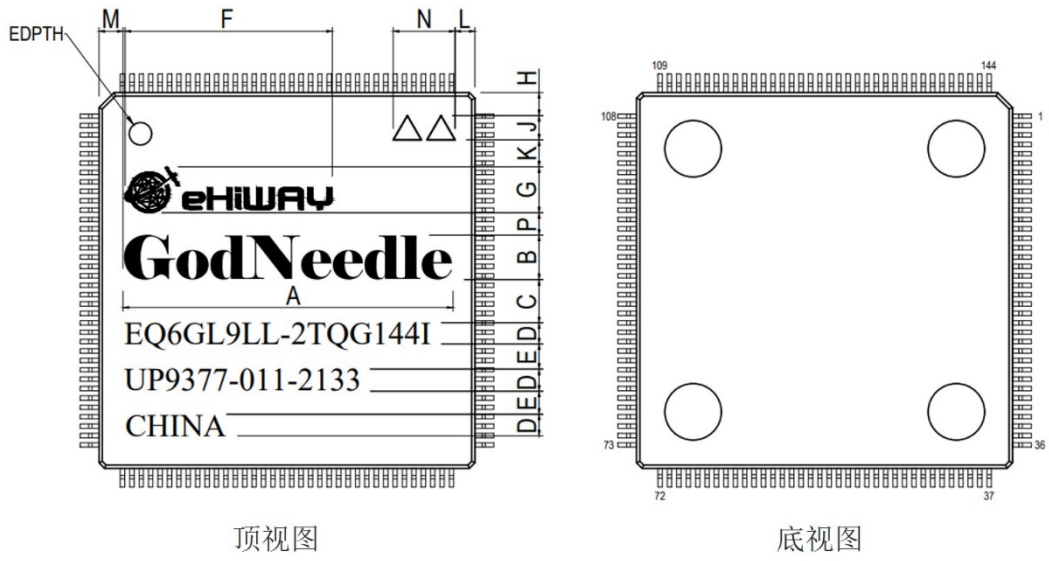


图 6 引出端排列示意图

GodNeedle-6 家族 FPGA 封装说明

附录 A

器件引出端及功能描述

封装管脚	管脚名称	BANK 编号
A1	GND	
A2	UIO_13_P02_B0_IXEN	B0
A3	UIO_37_P08_B1_DX4	B1
A4	UIO_39_P09_B1_DX6	B1
A5	UIO_43_P10_B1_DX7	B1
A6	UIO_197_P53_B7_REGSCAN	B7
A7	UIO_191_P51_B7_GCN_TOP_1	B7
A8	UIO_189_P50_B7_GCN_TOP_3	B7
A9	UIO_177_P47_B6_WI_DSP	B6
A10	GND	
B1	UIO_7_P00_B0_TRACK_SE	B0
B2	VCCO_0	
B3	UIO_38_N08_B1_DX5	B1
B4	UIO_40_N09_B1_VREF_FCLKRST	B1
B5	UIO_44_N10_B1_CDIRE	B1
B6	UIO_198_N53_B7_VREF_MXIN0	B7
B7	UIO_192_N51_B7_GCN_TOP_0	B7
B8	UIO_190_N50_B7_GCN_TOP_2	B7
B9	VCCO_6	
B10	UIO_171_P45_B6_SO_LAB	B6
C1	UIO_8_N00_B0_OSC_SL	B0
C2	UIO_14_N02_B0_MXSM	B0
C3	CIO_62_PROG_B	
C4	CIO_29_CFG_SL	
C5	VCCO_1	
C6	VCCO_7	
C7	TDI	
C8	TMS	
C9	UIO_178_N47_B6_SI_DSP	B6
C10	UIO_172_N45_B6_TEST_SCAN_I	B6
D1	UIO_9_P01_B0_SI_TRACK	B0
D2	CIO_3_SPI_AD	
D3	VCCAUX	
D4	CIO_30_INIT_B	
D5	VCCINT	
D6	GND	
D7	VCCINT	
D8	GND	

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封装管脚	管脚名称	BANK 编号
D9	TDO	
D10	UIO_173_P46_B6_TEST_DSP_I	B6
E1	UIO_10_N01_B0_VREF	B0
E2	CIO_4_DONE	
E3	GND	
E4	VCCINT	
E5	GND	
E6	VCCINT	
E7	CIO_135_TESTMODE	
E8	VCCAUX	
E9	TCK	
E10	UIO_174_N46_B6_VREF	B6
F1	UIO_67_P16_B2_D7	B2
F2	UIO_73_P18_B2_VREF_FAIL_H_O	B2
F3	CIO_33_FCS_B_O	
F4	CIO_139_BCERR	
F5	VCCINT	
F6	GND	
F7	VCCINT	
F8	GND	
F9	CIO_138_BUSY_DOUT	
F10	UIO_149_N39_B5_OSTATE4	B5
G1	UIO_68_N16_B2_D6	B2
G2	UIO_74_N18_B2_D3	B2
G3	CIO_34_FCS_B_I	
G4	VCCINT	
G5	GND	
G6	VCCINT	
G7	CIO_59_M2	
G8	VCCA	
G9	CIO_207_CCTL	
G10	UIO_148_P39_B5_VREF	B5
H1	UIO_69_P17_B2_D5	B2
H2	UIO_90_P23_B3_GCN_BOT_1	B3
H3	CIO_87_CCLK	
H4	CIO_106_D1	
H5	VCCO_3	
H6	VCCO_4	
H7	CIO_60_M1	
H8	CIO_61_M0	
H9	UIO_144_P38_B5_FRZEN_I	

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封装管脚	管脚名称	BANK 编号
H10	UIO_145_N38_B5_TOTDATA_I	
J1	UIO_70_N17_B2_D4	
J2	VCCO_2	
J3	CIO_134_SPI_DO	
J4	CIO_107_D0	
J5	UIO_95_N25_B3_RDWR_B	
J6	UIO_110_P28_B4_MXBC	
J7	UIO_112_P29_B4_MXAD3	
J8	UIO_114_P30_B4_MXAD5	
J9	VCCO_5	
J10	UIO_143_N37_B5_CLRBAREN_I	
K1	GND	
K2	UIO_91_N23_B3_GCN_BOT_0	
K3	UIO_92_P24_B3_VREF_SO_DSP0	
K4	UIO_93_N24_B3_WO_DSP0	
K5	UIO_94_P25_B3_MXWCLK	
K6	UIO_111_N28_B4_MXAC	
K7	UIO_113_N29_B4_MXAD4	
K8	UIO_115_N30_B4_MXAD6	
K9	UIO_142_P37_B5_TOTRST	
K10	GND	

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附录 B

器件引出端及功能描述

封装管脚	管脚名称	BANK 编号
A1	NC	
A2	VCCINT_57	
A3	UIO_53_P14_B1_MXEN0	B1
A4	UIO_49_P13_B1_FRZCLK	B1
A5	UIO_54_N14_B1_MXEN1	B1
A6	UIO_48_N12_B1_MXABR	B1
A7	UIO_39_P09_B1_DX6	B1
A8	VCCINT_35	
A9	VCCAUX_31	
A10	VCCINT_27	
A11	UIO_20_N05_B0_VREF	B0
A12	GND0_12_B0	
A13	UIO_19_P05_B0_REGRST	B0
A14	UIO_15_P03_B0_MXWR	B0
A15	UIO_13_P02_B0_IXEN	B0
A16	UIO_9_P01_B0_SI_TRACK	B0
B1	GNDINT_66	
B2	NC	
B3	VCCAUX_63	
B4	CIO_59_M2	
B5	GNDINT_58	
B6	GND0_52_B1	
B7	VCCO_41_B1	
B8	CIO_33_FCS_B_O	
B9	CIO_29_CFG_SL	
B10	UIO_23_P06_B0_DX0	B0
B11	UIO_16_N03_B0	B0
B12	UIO_10_N01_B0_VREF	B0
B13	GNDINT_6	
B14	UIO_7_P00_B0_TRACK_SE	B0
B15	CIO_4_DONE	
B16	NC	
C1	UIO_68_N16_B2_D6	B2
C2	NC	
C3	NC	
C4	CIO_62_PROG_B	
C5	UIO_56_N15_B1_MXRBD1	B1

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封装管脚	管脚名称	BANK 编号
C6	UIO_50_N13_B1_VREF	B1
C7	UIO_46_N11_B1	B1
C8	UIO_43_P10_B1_DX7	B1
C9	UIO_25_P07_B0_DX2	B0
C10	UIO_18_N04_B0	B0
C11	UIO_14_N02_B0_MXSM	B0
C12	UIO_8_N00_B0_OSC_SL	B0
C13	GND_AUX_1	
C14	CIO_2_TDI	
C15	NC	
C16	NC	
D1	GND_O_72_B2	
D2	NC	
D3	NC	
D4	NC	
D5	CIO_61_M0	
D6	CIO_60_M1	
D7	UIO_40_N09_B1_VREF_FCLKRST	B1
D8	UIO_37_P08_B1_DX4	B1
D9	CIO_30_INIT_B	
D10	GNDINT_28	
D11	CIO_3_SPI_AD	
D12	VCCO_11_B0	
D13	VCCAUX_0	
D14	NC	
D15	NC	
D16	UIO_204_N55_B7_SI_LAB	B7
E1	VCCINT_65	
E2	NC	
E3	NC	
E4	NC	
E5	GND_AUX_64	
E6	VCCO_51_B1	
E7	UIO_45_P11_B1	B1
E8	GNDINT_36	
E9	GND_AUX_32	
E10	GND_O_22_B0	
E11	UIO_17_P04_B0	B0
E12	NC	
E13	NC	

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封装管脚	管脚名称	BANK 编号
E14	NC	
E15	NC	
E16	NC	
F1	UIO_73_P18_B2_VREF_FAIL_H_O	B2
F2	UIO_69_P17_B2_D5	B2
F3	UIO_67_P16_B2_D7	B2
F4	NC	
F5	UIO_70_N17_B2_D4	B2
F6	UIO_55_P15_B1_MXRBD0	B1
F7	UIO_47_P12_B1	B1
F8	GNDO_42_B1	
F9	UIO_26_N07_B0_DX3	B0
F10	VCCO_21_B0	
F11	NC	
F12	NC	
F13	NC	
F14	VCCINT_205	
F15	CIO_207_CCTL	
F16	UIO_203_P55_B7_SO_TRACK	B7
G1	UIO_79_P21_B2_EN_BIST_I	B2
G2	UIO_75_P19_B2_D2	B2
G3	VCCO_71_B2	
G4	VCCO_81_B2	
G5	UIO_76_N19_B2_MBIST_RST_I	B2
G6	UIO_74_N18_B2_D3	B2
G7	UIO_38_N08_B1_DX5	B1
G8	UIO_44_N10_B1_CDIR	B1
G9	UIO_24_N06_B0_DX1	B0
G10	VCCO_193_B7	
G11	UIO_202_N54_B7_OSC_I	B7
G12	GNDO_200_B7	
G13	NC	
G14	UIO_201_P54_B7_MXIN1	B7
G15	NC	
G16	GNDO_194_B7	
H1	UIO_84_N22_B2_GCN_BOT_2	B2
H2	GNDO_82_B2	
H3	UIO_77_P20_B2_TESTM4K_I	B2
H4	UIO_83_P22_B2_GCN_BOT_3	B2
H5	VCCINT_85	

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封装管脚	管脚名称	BANK 编号
H6	UIO_80_N21_B2_VREF_MBIST_CLK_I	B2
H7	UIO_78_N20_B2_DONE_MBIST_O	B2
H8	CIO_34_FCS_B_I	
H9	UIO_189_P50_B7_GCN_TOP_3	B7
H10	UIO_198_N53_B7_VREF_MXIN0	B7
H11	UIO_197_P53_B7_REGSCAN	B7
H12	UIO_191_P51_B7_GCN_TOP_1	B7
H13	UIO_192_N51_B7_GCN_TOP_0	B7
H14	VCCO_199_B7	
H15	GNDINT_188	
H16	UIO_190_N50_B7_GCN_TOP_2	B7
J1	VCCAUX_88	
J2	GNDINT_86	
J3	VCCO_96_B3	
J4	UIO_90_P23_B3_GCN_BOT_1	B3
J5	GNDAX_89	
J6	UIO_95_N25_B3_RDWR_B	B3
J7	GND0_97_B3	
J8	CIO_87_CCLK	
J9	GNDAX_137	
J10	NC	
J11	NC	
J12	VCCINT_187	
J13	NC	
J14	NC	
J15	NC	
J16	NC	
K1	UIO_92_P24_B3_VREF_SO_DSP0	B3
K2	UIO_94_P25_B3_MXWCLK	B3
K3	UIO_99_N26_B3_MXAD0	B3
K4	UIO_93_N24_B3_WO_DSP0	B3
K5	UIO_98_P26_B3_VREF	B3
K6	UIO_100_P27_B3_MXAD1	B3
K7	UIO_91_N23_B3_GCN_BOT_0	B3
K8	GND0_127_B4	
K9	GND0_147_B5	
K10	GNDINT_141	
K11	NC	
K12	NC	
K13	vcca	

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封装管脚	管脚名称	BANK 编号
K14	NC	
K15	NC	
K16	NC	
L1	UIO_101_N27_B3_MXAD2	B3
L2	NC	
L3	GNDINT_103	
L4	NC	
L5	NC	
L6	NC	
L7	UIO_123_N33_B4_DXR D	B4
L8	UIO_129_N35_B4_TOTclk	B4
L9	UIO_145_N38_B5_TOTDATA_I	B5
L10	UIO_150_P40_B5_OSTATE3	B5
L11	UIO_158_P43_B5_VREF	B5
L12	NC	
L13	NC	
L14	NC	
L15	NC	
L16	NC	
M1	NC	
M2	NC	
M3	NC	
M4	NC	
M5	NC	
M6	UIO_120_P32_B4_DXBC	B4
M7	UIO_125_N34_B4_DXAC	B4
M8	CIO_135_TESTMODE	
M9	CIO_139_BCERR	
M10	UIO_148_P39_B5_VREF	B5
M11	UIO_154_P42_B5_PSTATE4	B5
M12	VCCAUX_167	
M13	NC	
M14	NC	
M15	NC	
M16	gnda	
N1	VCCINT_102	
N2	NC	
N3	NC	
N4	VCCAUX_104	
N5	UIO_114_P30_B4_MXAD5	B4

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封装管脚	管脚名称	BANK 编号
N6	CIO_107_D0	
N7	UIO_131_N36_B4_ADEN_I	B4
N8	GNDINT_133	
N9	VCCINT_140	
N10	UIO_143_N37_B5_CLRBAREN_I	B5
N11	GNDINT_163	
N12	CIO_164_TMS	
N13	NC	
N14	NC	
N15	NC	
N16	NC	
P1	NC	
P2	NC	
P3	CIO_106_D1	
P4	GND_AUX_105	
P5	UIO_111_N28_B4_MXAC	B4
P6	GND_O_117_B4	
P7	UIO_121_N32_B4_DXBR	B4
P8	UIO_128_P35_B4_VREF	B4
P9	VCCO_146_B5	
P10	UIO_149_N39_B5_OSTATE4	B5
P11	UIO_153_N41_B5_OSTATE0	B5
P12	UIO_159_N43_B5_PSTATE2	B5
P13	CIO_165_TCK	
P14	NC	
P15	NC	
P16	NC	
R1	NC	
R2	VCCINT_108	
R3	UIO_110_P28_B4_MXBC	B4
R4	GNDINT_109	
R5	UIO_113_N29_B4_MXAD4	B4
R6	UIO_119_N31_B4_DXAR	B4
R7	VCCO_126_B4	
R8	VCCINT_132	
R9	VCCAUX_136	
R10	UIO_144_P38_B5_FRZEN_I	B5
R11	UIO_155_N42_B5_PSTATE3	B5
R12	UIO_161_N44_B5_PSTATE0	B5
R13	VCCINT_162	

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封装管脚	管脚名称	BANK 编号
R14	CIO_166_TDO	
R15	NC	
R16	NC	
T1	UIO_112_P29_B4_MXAD3	B4
T2	VCCO_116_B4	
T3	UIO_118_P31_B4_VREF	B4
T4	UIO_122_P33_B4_DXWR	B4
T5	UIO_115_N30_B4_MXAD6	B4
T6	UIO_124_P34_B4_DXSM	B4
T7	UIO_130_P36_B4_CLRSRMEN_I	B4
T8	CIO_134_SPI_DO	
T9	CIO_138_BUSY_DOUT	
T10	UIO_142_P37_B5_TOTRST	B5
T11	UIO_151_N40_B5_OSTATE2	B5
T12	GND0_157_B5	
T13	UIO_152_P41_B5_OSTATE1	B5
T14	VCCO_156_B5	
T15	UIO_160_P44_B5_PSTATE1	B5
T16	NC	

GodNeedle-6 家族 FPGA 封装说明

附录 C

器件引出端及功能描述

封装管脚	管脚名称	BANK 编号
P1	UIO_7_P00_B0_TRACK_SE	B0
P2	UIO_8_N00_B0_OSC_SL	B0
P3	UIO_9_P01_B0_SI_TRACK	B0
P4	UIO_10_N01_B0_VREF	B0
P5	VCCO_11_B0	B0
P6	UIO_15_P03_B0_MXWR	B0
P7	UIO_16_N03_B0	B0
P8	UIO_19_P05_B0_REGRST	B0
P9	UIO_20_N05_B0_VREF	B0
P10	VCCO_21_B0	B0
P11	UIO_25_P07_B0_DX2	B0
P12	UIO_26_N07_B0_DX3	B0
P13	VCCINT_27	
P14	CIO_29_CFG_SL	
P15	CIO_30_INIT_B	
P16	VCCAUX_31	
P17	CIO_33_FCS_B_O	
P18	GND	
P19	CIO_34_FCS_B_I	
P20	UIO_37_P08_B1_DX4	B1
P21	UIO_38_N08_B1_DX5	B1
P22	UIO_39_P09_B1_DX6	B1
P23	UIO_40_N09_B1_VREF_FCLKRST	B1
P24	VCCO_41_B1	B1
P25	UIO_43_P10_B1_DX7	B1
P26	UIO_44_N10_B1_CDIR	B1
P27	UIO_47_P12_B1	B1
P28	UIO_48_N12_B1_MXABR	B1
P29	UIO_49_P13_B1_FRZCLK	B1
P30	UIO_50_N13_B1_VREF	B1
P31	VCCO_51_B1	B1
P32	UIO_55_P15_B1_MXRBD0	B1
P33	UIO_56_N15_B1_MXRBD1	B1
P34	VCCINT_57	
P35	CIO_59_M2	
P36	CIO_60_M1	
P37	CIO_61_M0	
P38	CIO_62_PROG_B	
P39	VCCAUX_63	

GodNeedle-6 家族 FPGA 封装说明

封装管脚	管脚名称	BANK 编号
P40	UIO_67_P16_B2_D7	B2
P41	UIO_68_N16_B2_D6	B2
P42	UIO_69_P17_B2_D5	B2
P43	UIO_70_N17_B2_D4	B2
P44	VCCO_71_B2	B2
P45	UIO_73_P18_B2_VREF_FAIL_H_O	B2
P46	UIO_74_N18_B2_D3	B2
P47	UIO_75_P19_B2_D2	B2
P48	UIO_76_N19_B2_MBIST_RST_I	B2
P49	UIO_77_P20_B2_TESTM4K_I	B2
P50	UIO_78_N20_B2_DONE_MBIST_O	B2
P51	UIO_79_P21_B2_EN_BIST_I	B2
P52	UIO_80_N21_B2_VREF_MBIST_CLK_I	B2
P53	VCCO_81_B2	B2
P54	GND	
P55	UIO_83_P22_B2_GCN_BOT_3	B2
P56	UIO_84_N22_B2_GCN_BOT_2	B2
P57	VCCINT_85	
P58	CIO_87_CCLK	
P59	VCCAUX_88	
P60	UIO_90_P23_B3_GCN_BOT_1	B3
P61	UIO_91_N23_B3_GCN_BOT_0	B3
P62	UIO_92_P24_B3_VREF_SO_DSP0	B3
P63	UIO_93_N24_B3_WO_DSP0	B3
P64	UIO_94_P25_B3_MXWCLK	B3
P65	UIO_95_N25_B3_RDWR_B	B3
P66	VCCO_96_B3	
P67	UIO_98_P26_B3_VREF	
P68	UIO_99_N26_B3_MXAD0	
P69	UIO_100_P27_B3_MXAD1	
P70	UIO_101_N27_B3_MXAD2	
P71	VCCAUX_104	
P72	CIO_106_D1	
P73	CIO_107_D0	
P74	VCCINT_108	
P75	UIO_112_P29_B4_MXAD3	B4
P76	UIO_113_N29_B4_MXAD4	B4
P77	UIO_114_P30_B4_MXAD5	B4
P78	UIO_115_N30_B4_MXAD6	B4
P79	VCCO_116_B4	B4
P80	UIO_120_P32_B4_DXBC	B4

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封装管脚	管脚名称	BANK 编号
P81	UIO_121_N32_B4_DXBR	B4
P82	UIO_122_P33_B4_DXWR	B4
P83	UIO_123_N33_B4_DXRDR	B4
P84	UIO_124_P34_B4_DXSM	B4
P85	UIO_125_N34_B4_DXAC	B4
P86	VCCO_126_B4	B4
P87	UIO_130_P36_B4_CLRSRMEN_I	B4
P88	UIO_131_N36_B4_ADEN_I	B4
P89	CIO_134_SPI_DO	
P90	GND	
P91	CIO_135_TESTMODE	
P92	VCCAUX_136	
P93	CIO_138_BUSY_DOUT	
P94	VCCINT_140	
P95	UIO_142_P37_B5_TOTRST	B5
P96	UIO_143_N37_B5_CLRBAREN_I	B5
P97	UIO_144_P38_B5_FRZEN_I	B5
P98	UIO_145_N38_B5_TOTDATA_I	B5
P99	VCCO_146_B5	B5
P100	UIO_148_P39_B5_VREF	B5
P101	UIO_149_N39_B5_OSTATE4	B5
P102	UIO_152_P41_B5_OSTATE1	B5
P103	UIO_153_N41_B5_OSTATE0	B5
P104	UIO_154_P42_B5_PSTATE4	B5
P105	UIO_155_N42_B5_PSTATE3	B5
P106	VCCO_156_B5	B5
P107	UIO_160_P44_B5_PSTATE1	B5
P108	UIO_161_N44_B5_PSTATE0	B5
P109	VCCINT_162	
P110	CIO_164_TMS	
P111	CIO_165_TCK	
P112	CIO_166_TDO	
P113	VCCAUX_167	
P114	VCCINT_169	
P115	UIO_171_P45_B6_SO_LAB	B6
P116	UIO_172_N45_B6_TEST_SCAN_I	B6
P117	UIO_173_P46_B6_TEST_DSP_I	B6
P118	UIO_174_N46_B6_VREF	B6
P119	VCCO_175_B6	B6
P120	UIO_177_P47_B6_WI_DSP	B6
P121	UIO_178_N47_B6_SI_DSP	B6

GodNeedle-6 家族 FPGA 封装说明

封装管脚	管脚名称	BANK 编号
P122	UIO_179_P48_B6_SE_DSP	B6
P123	UIO_180_N48_B6_VREF_WSF_DSP	B6
P124	PLL_GNDA	
P125	PLL_VCCA	
P126	GND	
P127	VCCINT_187	
P128	UIO_189_P50_B7_GCN_TOP_3	B7
P129	UIO_190_N50_B7_GCN_TOP_2	B7
P130	UIO_191_P51_B7_GCN_TOP_1	B7
P131	UIO_192_N51_B7_GCN_TOP_0	B7
P132	VCCO_193_B7	B7
P133	UIO_197_P53_B7_REGSCAN	B7
P134	UIO_198_N53_B7_VREF_MXIN0	B7
P135	VCCO_199_B7	B7
P136	UIO_201_P54_B7_MXIN1	B7
P137	UIO_202_N54_B7_OSC_I	B7
P138	UIO_203_P55_B7_SO_TRACK	B7
P139	UIO_204_N55_B7_SI_LAB	B7
P140	VCCINT_205	
P141	VCCAUX_0	
P142	CIO_2_TDI	
P143	CIO_3_SPI_AD	
P144	CIO_4_DONE	